PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	: Patricia B. SMITH et al.	Confirmation No.:	3087
Application Number	: 10/647,985		
Filed	: August 26, 2003		
Title	: POST-ETCH CLEAN PROCESS FOR POROUS LOW DIELECTRIC CONSTANT MATERIALS		
TC/Art Unit	: 1792		
Examiner:	: Zeinab El Arini		
Docket No.	: TI-33260 (0025.0184)		
Customer No.	: **23494**		

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUBMISSION OF BRIEF ON APPEAL

Please enter this Appeal Brief in response to the Examiner's Final Office Action mailed January 10, 2008 and the Applicants' Notice of Appeal filed May 12, 2008.

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APPLICANTS' BRIEF ON APPEAL

I. REAL PARTY IN INTEREST

The Applicants, Patricia Beauregard Smith, Heungsoo Park, and Eden Zielinski, have assigned their interest in this application to Texas Instruments, Inc. as evidenced by the recordation on August 26, 2003 at reel/frame 014448/0702.

II. RELATED APPEALS AND INTERFERENCES

Appellants, appellants' legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-23 have been presented during prosecution of the application under appeal;

Claims 7, 16, and 19 have been canceled; and

Claims 1-6, 8-15, 17, 18, and 20-23 are pending, rejected, and appealed.

IV. STATUS OF THE AMENDMENTS

No amendment has been filed by the applicants for the above-captioned case subsequent to the final rejection of January 10, 2008.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As set forth in claim 1, a method for cleaning a wafer is illustrated in FIG. 1 (see, e.g., specification, page 2, ¶[0006]).

The method comprises patterning a via 106 or a trench 108, or both, in a porous, low-k dielectric layer 102 overlying the wafer 100 as illustrated in FIG. 1 (see, e.g., page 3 ¶[0011] and page 4, ¶[0012]). A polymer residue is then cleaned from the surfaces of the patterned dielectric layer 102 using a wet clean solvent as illustrated in FIG. 1 (see e.g., page 3 ¶[0011] and page 5 ¶[0014]). A non-plasma anneal is then performed on the patterned dielectric layer to remove a component of the solvent prior to a metal 110 deposition, wherein the anneal comprises a low pressure anneal from about one atmosphere of pressure to substantial vacuum as illustrated in FIG. 1 (see, e.g., page 6, ¶¶[0015] and [0017], and page 7 ¶[0020]). After an anneal duration of about six minutes or less, the anneal is stopped (see, e.g., page 6, ¶[0017]).

As recited in claim 20, a method for removing volatile cleanser compounds from a post-etch substrate 100 is disclosed (see, e.g., page 5, ¶[0013] and page 6, ¶[0017]). A plasma strip of an exposed low-k dielectric material 102 is performed to remove a photoresist residue after an etching of the material (see, e.g., page 5, ¶[0013]). A wet clean process is then performed using a fluorine-based solvent to remove a polymer residue of the plasma strip from the material, as illustrated in FIG. 1 (see, e.g., page 5, ¶[0014]). The method further comprises performing an anneal at a pressure of about one atmosphere or less and a temperature of between about 250°C and about 300°C after the wet clean process and prior to a metal barrier deposition to remove a component of the fluorine-based solvent from the material (see, e.g., page 6, ¶[0017],

and page 7, ¶[0019]). The anneal is exclusive of an application of a plasma generated from one or more of: a radio-frequency (RF) radiation and a microwave radiation, as illustrated in FIG. 1 (see, e.g., page 5, ¶[0013]). After an anneal duration of about six minutes or less, the anneal is stopped (see, e.g., page 6, ¶[0017]).

As recited in claim 21, a method used during fabrication of a semiconductor device is disclosed. The method comprises patterning a via 106 or trench 108, or both, in a low-k dielectric layer 102 comprising organosilicate glass (OSG) (see, e.g., FIG. 1 and page 3, ¶[0011]) and cleaning a polymer residue from a surface of the patterned dielectric layer using a wet clean solvent as illustrated in FIG. 1 (see e.g., page 3 ¶[0011] and page 5 ¶[0014]). A non-plasma anneal is performed on the patterned dielectric layer at a temperature of about 250 °C for a duration of about 45 seconds (see, e.g., page 6, ¶[0015]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 8, 9, 11, 12, 15, 18, and 21-23 stand rejected under 35 USC §103(a) as being unpatentable over Chang (5,643,407, hereinafter "Chang '407"). Claims 5, 6, and 17 stand rejected under 35 USC §103(a) as being unpatentable over Chang '407 in combination with Nguyen et al. (2003/0104320). Claims 2-4, 10, 13, and 14 stand rejected as being unpatentable over Chang '407 in combination with Nguyen et al. '320 as applied to claims 5, 6, and 17, and further in view of Chang et al. (2003/0008518, hereinafter "Chang '518"), Chiu et al. (6,107,202), and Akino et al. (6,417,108). Claim 20 stands rejected under 35 USC §103(a) as being unpatentable over Smith et al. (2002/0058397).

VII. ARGUMENT

Rejection of claims 1, 8, 9, 11, 12, 15, and 18 under 35 USC §103(a) over Chang (5,643,407)

Claims 1, 8, 9, 11, 12, 15, and 18 stand rejected under 35 USC §103(a) over Chang '407. A reversal of the rejection is respectfully requested for at least the following reasons.

Claim 1 recites a method of cleaning a wafer including, among other things, cleaning a polymer residue from surfaces of the patterned dielectric layer using a wet clean solvent, performing a non-plasma anneal on the patterned dielectric layer to remove a component of the solvent prior to a metal deposition and, after an anneal duration of about six minutes or less, stopping the anneal.

The Examiner recognizes that Chang '407 fails to disclose the claimed anneal duration, but states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the anneal duration to obtain optimum results. Applicants submit, however, that one of ordinary skill in the art at the time the invention was made would not have optimized the anneal duration to remove the component of the solvent, at least because the art failed to recognize that removal of the component of the solvent was a result-effective variable. Assuming that the process of Chang '407 has not already been optimized, optimization would not result in the claimed "anneal duration of six minutes or less," at least because Chang's process would be optimized to remove moisture, not a component of the solvent as claimed.

Chang '407 discloses a method comprising etching a via through first 14 and second 18 silicon oxide layers and a silicate or siloxane coating 16 (FIG. 3) using a photoresist layer and a wet etch such as a buffered oxide etch. The photoresist layer is removed using a wet strip, for example using hydroxylamine, followed by an optional O_2 plasma ashing, which generates moisture. Next, a "critical" two-step spin-on-glass (SOG) treatment is performed by baking the wafer in a vacuum of less than 10 mTorr at a temperature of between 250° and 350°C for between about 20 and 40 minutes. The vacuum bake removes moisture from the exposed SOG layer generated during the decomposition of the organic spin-on-glass material during O_2 ashing of the photoresist (col. 2, line 45 to col. 3, line 36).

It is submitted that claim 1 is allowable over Chang '407 for at least the recitation of "performing a non-plasma anneal...to remove a component of the solvent." In contrast to this claim 1 element, the process of Chang '407 is performed to remove "moisture" resulting from decomposition of the SOG layer, not to remove a component of the solvent as currently claimed. Paragraphs [0015] through [0017] of the current specification discuss the inventors' discovery of the cause of the failure, which was different than that originally assumed, and their method for correcting the failure, accomplished by removing the component of the solvent from the dielectric film. Thus, Applicants submit that claim 1, which recites "performing a non-plasma anneal on the patterned dielectric layer to remove a component of the [wet clean] solvent" is allowable over Chang '407, which performs a baking step to remove moisture generated during an O_2 plasma ashing.

The term "moisture" is generally recognized to be water or water vapor. At ¶3, lines 22-25, Chang discusses that the "moisture" occurs from decomposition of an "alkyl" (i.e. a carbon-hydrogen radical) from the organic SOG layer in an O_2 plasma. Thus it appears that the "moisture" of Chang '407 is water or water vapor resulting from the combination of hydrogen from the decomposed alkyl and oxygen from the O_2 plasma. A process to remove water vapor would be different than a process "to remove a component of the [wet clean] solvent" as presently claimed.

More specifically, claim 1 recites "after an anneal duration of about six minutes or less, stopping the anneal." The claimed anneal time is performed "to remove the component of the solvent," but the baking process of Chang '407, which is deemed "critical" and is performed to remove moisture, requires "a temperature of between about 250° to 350°C for between about 20 to 40 minutes" (col. 3, lines 34, 35). Thus the claimed process performed "to remove a component of the solvent" and is performed "for about six minutes or less" is novel and nonobvious over the process of Chang '407, which is performed to remove moisture from decomposition of the SOG layer.

It is well established that excessive heat is detrimental to semiconductor structures during processing and that process engineers attempt to minimize the exposure of the semiconductor wafer to heat to remain within a "thermal budget." Chang '407 recites performing the baking step for 20 to 40 minutes, and thus it appears that about 20 minutes would be a minimum baking time to practice the method of Chang '407. To conserve the thermal budget, Chang '407 would have minimized the baking step duration, and thus it is submitted that the anneal time currently claimed is novel and nonobvious over the method of Chang '407.

The Examiner rejects claim 1 over Chang '407 and states that "it would have been obvious to a person having ordinary skill in the art at the time the invention was made to adjust the anneal duration to obtain optimum results, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art" and that "the time for annealing depends on the amount of moisture to be removed from the surface." However, optimizing Chang '407 would involve optimizing the process to remove moisture, not "to remove a component of the solvent" as claimed. At ¶¶15-17, the current specification discusses the inventors' discovery of the cause of the failure, which was different than that originally assumed, and their method for correcting the failure, accomplished by removing the component of the solvent from the dielectric film. Chang '407 does not recognize the component of the solvent as a problem. Because Chang '407 is attempting to remove moisture generated from decomposition of the SOG layer, not a component of the solvent as claimed, an optimization by Chang '407 would not result in the claimed invention.

It is submitted that Chang '407 would have listed a minimum baking time sufficient to remove a minimum amount of moisture to minimize the thermal budget. Thus optimization of the process of Chang '407 to remove moisture would not result in the invention as claimed wherein the anneal is stopped "after an anneal duration of about six minutes or less," at least because with the claimed invention the anneal is performed "to remove a component of the solvent." The baking step duration of Chang '407 is not a result-effective variable with respect to the invention as claimed, at least because different materials are targeted for removal. Therefore, the processes are different, at least because different materials are being targeted for removal, which

results in the duration for the claimed method being substantially less to remove the different material than that discussed by Chang '407.

Thus it is submitted that Chang '407 fails to expressly or impliedly suggest the claimed invention, and that the "optimization" of Chang '407 would not result in the invention as claimed and does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to be obvious in light of the teachings of the references as required (MPEP §706.02(j)). Claim 1, and rejected claims 8, 9, 11, 12, 15, and 18 which depend therefrom, are allowable over Chang '407 under 35 USC §103(a). For at least the foregoing reasons, the rejection over Chang '407 is improper and the Examiner's rejection is respectfully traversed.

Rejection of claims 21-23 under 35 USC §103(a) over Chang (5,643,407)

Claims 21-23 stand rejected under 35 USC §103(a) over Chang '407. A reversal of the rejection is respectfully requested for at least the following reasons.

Claim 21 recites a method comprising patterning a via or a trench, or both, in a low-k dielectric layer comprising organosilicate glass (OSG), cleaning a polymer residue from a surface of the patterned dielectric layer using a wet clean solvent, and performing a non-plasma anneal on the patterned dielectric layer at a temperature of about 250°C for a duration of about 45 seconds.

Chang '407 recites a method as discussed relative to the rejection of claim 1, including baking the wafer at a temperature of between about 250° and 350°C for

between about 20 and 40 minutes. Chang '407 deems the two step process which includes the baking step as "critical" (col. 3, lines 30-36).

Claim 21 is allowable over Chang '407 at least for its recitation of "performing a non-plasma anneal on the patterned dielectric layer at a temperature of about 250°C for a duration of about 45 seconds." Chang '407 recites that the "critical" two-step process, which includes baking the wafer in a vacuum at a temperature of between 250° and 350°C, requires between about 20 and 40 minutes. A duration of "about 45 seconds" is less than 1/26 of the minimum duration recited by Chang '407. It is submitted that Chang '407 would have minimized the time required to remove the moisture so that the thermal budget would be conserved as discussed relative to the rejection of claim 1. Thus the invention as recited in claim 21 is allowable over Chang '407, at least because Chang '407 fails to teach or suggest "performing a non-plasma anneal on the patterned dielectric layer at a temperature of about 250 °C for a duration of about 45 seconds" as presently claimed, and as required for proper rejection under 35 USC §103(a).

The Examiner rejects claim 21 over Chang '407 and states that "it would have been obvious to a person having ordinary skill in the art at the time the invention was made to adjust the anneal duration to obtain optimum results, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art" and that "the time for annealing depends on the amount of moisture to be removed from the surface." However, optimizing Chang '407 would involve optimizing the process to remove moisture. At ¶¶15-17, the current specification discusses the inventors' discovery of the cause of the failure, which was different than that originally assumed, and their method for correcting the failure, accomplished by removing the

component of the solvent from the dielectric film. Chang '407 does not recognize the component of the solvent as a problem. Because Chang '407 is attempting to remove moisture generated from decomposition of the SOG layer, an optimization by Chang '407 would not result in the claimed invention. While claim 21 does not specify the material being targeted for removal, it is submitted that an optimization of Chang '407 would not result in a baking duration of "about 45 seconds" as claimed, at least because Chang '407 is targeting moisture for removal which, according to Chang' 407, takes between 20 and 40 minutes at 250°C to 350°C.

It is submitted that Chang '407 would have listed a minimum baking time sufficient to remove a minimum amount of moisture to minimize the thermal budget. Thus optimization of the process of Chang '407 to remove moisture would not result in the invention as claimed wherein the anneal is stopped after "about 45 seconds."

Claim 23 is further allowable over Chang '407. Claim 23 recites the method of claim 21 and further comprises "performing the non-plasma anneal to remove a component of the wet clean solvent." This is in contrast to the process of Chang '407, which is performed to remove moisture generated during decomposition of a SOG layer resulting from an O_2 plasma (col. 3, lines 22-36). It is not evident that such a process would remove the moisture as required by Chang '407, and in any case Chang '407 performs the process to remove moisture generated by the O_2 plasma and not a component of the wet clean solvent. Thus claim 23 is further allowable over Chang '407, which fails to teach or suggest "performing the non-plasma anneal to remove a component of the wet clean solvent."

Thus claims 21-23 are allowable over Chang '407, and the Examiner's rejection of the claims is respectfully traversed.

Rejection of claims 5, 6, and 17 under 35 USC §103(a) over Chang (5,643,407) in combination with Nguyen et al. (2003/0104320)

Claims 5, 6, and 17 stand rejected under 35 USC §103(a) over Chang '407 in combination with Nguyen et al. (2003/0104320). A reversal of the rejection is respectfully requested for the following reasons.

Claims 5, 6, and 17 recite through claim 1 from which they depend, among other things, a method comprising cleaning a polymer residue from surfaces of a patterned dielectric layer using a wet clean solvent, performing a non-plasma anneal on the patterned dielectric layer to remove a component of the solvent, and after an anneal duration of about six minutes or less, stopping the anneal.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must expressly or impliedly suggest all the claim limitations. However, the combination of references do not appear to teach or suggest the recitations of the rejected claims.

Chang '407 discloses a method comprising etching a dielectric layer using a photoresist layer as a pattern, removing the photoresist using a wet strip followed by an optional oxygen plasma ashing to ensure all the photoresist residue is removed, vacuum baking the wafer at a pressure of 10 mTorr or less and a temperature of between about 250°C to about 350°C for a duration of between about 20 to 40 minutes in a nitrogen ambient to remove moisture, and performing a nitrogen plasma treatment to convert the organic dielectric to an inorganic dielectric (col. 3, lines 13-48).

Nguyen et al. is cited in the rejection of dependent claims 5, 6, and 17 for its description of conventional semiconductor processing methods, specifically that the

conventional photoresist removal sequence typically consists of a dry strip using oxygen to remove the bulk of the photoresist layer followed by a wet clean process to remove the residues and metal contaminants, and that the conventional sequence further includes an anneal step to remove any moisture resulting from the wet strip (¶7).

While the Examiner has cited Nguyen to teach photoresist removal using both a dry strip process and a wet clean process, it should be noted that Chang '407 recites, subsequent to etching the via, removing the photoresist mask using a wet strip such as hydroxylamine followed by an O_2 plasma ashing (col. 3, lines 19-27). The ashing process decomposes an alkyl in the spin-on-glass dielectric which results in moisture formation.

As discussed relative to previous rejections *supra*, it is well established that excessive heat is detrimental to semiconductor structures during processing and that process engineers attempt to minimize the exposure of the semiconductor wafer to heat to remain within a "thermal budget." Chang '407 recites performing the baking step for 20 to 40 minutes (col. 3, line 24), and thus it appears that 20 minutes would be a minimum baking time to practice the method of Chang '407. To conserve the thermal budget, Chang '407 would have minimized the anneal duration. Moreover, Chang '407 states that this baking step is part of a "critical" process of the invention (col. 3, lines 30-33).

Claims 5, 6, and 17 of the present application are allowable at least for depending from an allowable base claim, specifically at least the claim 1 recitation that the anneal is stopped after a duration of about six minutes. Because a minimum of 20 minutes is a "critical" requirement of Chang '407 as discussed above, and therefore a

requirement for the combination of Chang '407 and Nguyen as applied by the Examiner, all of the claim limitations are not taught or suggested by the combination of references as required for proper rejection under 35 USC §103(a).

Further, Chang '407 discloses a method performed to remove moisture generated during decomposition of the organic spin-on-glass material during O_2 ashing of the photoresist (col. 3, lines 30-36). Claim 1 of the present application through which claims 5, 6, and 17 depend recites "performing a non-plasma anneal...*to remove a component of the solvent.*" Chang '407's process is performed to remove moisture, not to remove a component of the solvent. Optimization of Chang '407 and Nguyen would result in optimization to remove moisture generated from decomposition of SOG, not for removal of a component of the solvent. Chang '407 does not recognize the component of the solvent being a problem, and it is not the material being targeted for removal. Paragraphs [0015] through [0017] of the current specification discuss the inventors' discovery of the cause of the failure, which was different than that originally assumed, and their method for correcting the failure, accomplished by removing the component of the solvent from the dielectric film. It is submitted that optimization for moisture removal would not result in a baking duration of six minutes or less as claimed.

Additionally, Nguyen teaches a method for removing a photoresist which eliminates the need for a process comprising a wet clean step (¶[0010]). The Examiner has cited the background material of Nguyen to teach conventional photoresist removal using both a wet clean and a dry strip as a conventional process. As discussed above, Chang '407 itself teaches photoresist removal using both a dry strip and a wet clean (col. 3, lines 19-27). Thus it appears that combining Chang '407 and Nguyen would result in a photoresist removal process which eliminates the need for a wet clean.

However, the claim 1 method comprises "cleaning a polymer residue from surfaces of the patterned dielectric layer using a wet clean solvent." A combination of Chang '407 and Nguyen, therefore, teaches away from the present invention as claimed, and claims 5, 6, and 17 which depend from claim 1 are allowable over the combination of Chang '407 and Nguyen.

Because Chang '407 and Nguyen fail to teach or suggest every feature of the recited method, for example performing the process to remove a component of the solvent and an anneal duration of six minutes or less as discussed above, claims 5, 6, and 17 are allowable under 35 USC §103(a) for at least this reason, and the Examiner's rejection is respectfully traversed.

Rejection of claims 2-4, 10, 13, and 14 under 35 USC §103(a) over Chang (5,643,407) in combination with Nguyen et al. (2003/0104320) and further in view of Chang et al. (2003/0008518), Chiu et al. (6,107,202), and Akino et al. (6,417,108)

Claims 2-4, 10, 13, and 14 stand rejected under 35 USC §103(a) over Chang '407 in combination with Nguyen as applied to claims 5, 6, and 17, and further in view of Chang (2003/0008518, hereinafter "Chang '518), Chiu et al. (6,107,202), and Akino et al (6,417,108).

Chang '407 and Nguyen recite the disclosure discussed *supra*. With regard to claim 2, Chang '518 recites MSQ as a low-k dielectric (claim 14). With regard to claim 4, Chiu '202 recites DMAC (col. 8, last line).

As discussed *supra* relative to the rejection of the claims over a combination of Chang '407, and a combination of Chang '407 and Nguyen '320, and for similar reasons, the combination of references fail to teach or suggest that the anneal is

stopped after a duration of about six minutes, and the disclosure of Chang '407 requires a minimum duration of 20 minutes. Further, Chang's process is performed to remove moisture generated from the decomposition of the organic spun-on-glass, not to remove a component of the solvent as recited in claim 1 from which the rejected claims depend. Optimization of the cited process would not result in the claimed anneal duration, at least because the claimed process recites a different target material and Chang '407 does not recognize the component of the solvent as a failure mode. Because all of the claim limitations are not taught or suggested by the combination of references as required for proper rejection under 35 USC §103(a), rejected claims 2-4, 10, 13, and 14 are therefore allowable for at least this reason, and the rejection is respectfully traversed.

Rejection of claim 20 under 35 USC §103(a) over Smith et al. (2002/0058397)

Claim 20 has been rejected under 35 USC §103(a) as being unpatentable over Smith et al. (US Pub. 2002/0058397).

Claim 20 as recites performing an anneal at a pressure of about one atmosphere or less and a temperature of between about 250°C and about 300°C after a wet clean process and, after an anneal duration of about six minutes or less, stopping the anneal.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a single reference, the reference must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. See, e.g., In Re Dow Chemical,

5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and In re Keller, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

In claims 1-4, Smith '397 recites subjecting the semiconductor wafer to a plasma so as to remove the photoresist layer, removing the polymeric residue using a process comprising a wet etch chemistry, and subjecting the semiconductor wafer to an annealing step to remove any excess fluid from action of the wet etch chemistry on the semiconductor wafer. In ¶27, Smith '397 discloses that the anneal is a "low temperature anneal" which "may be on the order of 60°C." Smith appears to be silent with regard to a pressure applied during the anneal, and also fails to discuss duration.

Smith et al. thus fails to teach or suggest at least the claim 20 recitations of "performing an anneal at a pressure of about one atmosphere or less," as well as "a temperature of between about 250°C and about 300°C" and further "after an anneal duration of about six minutes or less, stopping the anneal." The claimed invention recites the temperature of between "about 250°C and about 300°C," while Smith recites a "low temperature" anneal and suggests 60°C.

Smith thus fails to teach or suggest all the recitations of claim 20 as required for proper rejection under 35 USC §103(a), and thus claim 20 is allowable over Smith. Therefore, the Examiner's rejection of claim 20 under 35 USC §103(a) over Smith is respectfully traversed.

VIII. Conclusion

For the foregoing reasons, the applicants submit that claims 1-6, 8-15, 17, 18, and 20-23 are clearly not anticipated by the disclosure of the cited references, which do not render the method of the applicants' invention obvious. Accordingly, applicants respectfully request the reversal of the Examiner's rejection of claims 1-6, 8-15, 17, 18, and 20-23. This is believed to be a complete and proper response to the Final Office Action, responding to every ground of rejection stated by the Examiner. All grounds of rejection in the Final Office Action of January 10, 2008 are respectfully traversed.

Please grant any extensions of time required to enter this response and charge any additional required fees to Texas Instruments' deposit account 20-0668.

Respectfully submitted,

Dated: June 16, 2008

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Claims Appendix

1. (previously presented) A method for cleaning a wafer, comprising:

patterning a via or a trench, or both, in a porous, low-k dielectric layer overlying the wafer;

cleaning a polymer residue from surfaces of the patterned dielectric layer using a wet clean solvent;

performing a non-plasma anneal on the patterned dielectric layer to remove a component of the solvent prior to a metal deposition, wherein the anneal comprises a low pressure anneal from about one atmosphere of pressure to substantial vacuum; and

after an anneal duration of about six minutes or less, stopping the anneal.

2. (previously presented) The method of claim 1, wherein the dielectric layer comprises at least one of: an organosilicate glass (OSG), a methylsilsesquioxane (MSQ) dielectric material, a fluorine-doped silicate glass (FSG), and a silicon-dioxide (SiO2).

3. (previously presented) The method of claim 1, wherein the wet clean solvent comprises an acid.

4. (previously presented) The method of claim 3, wherein the component comprises dimethyl acetamide (DMAC).

5. (previously presented) The method of claim 1, further comprising: performing a dry clean of the patterned dielectric layer to remove a photoresist, prior to cleaning the polymer residue.

6. (previously presented) The method of claim 5, wherein the dry clean comprises a plasma including at least one of: hydrogen, oxygen and an inert gas.

7. (canceled)

8. (previously presented) The method of claim 1, wherein the low-pressure anneal is performed in substantially a vacuum.

9. (previously presented) The method of claim 1, wherein the anneal comprises a high-temperature anneal.

10. (previously presented) The method of claim 9, wherein the high-temperature anneal is performed at a higher temperature than a boiling point of the component.

11. (previously presented) The method of claim 9, wherein the high temperature anneal is performed at a temperature less than or equal to 300 degrees Celsius.

12. (previously presented) The method of claim 9, wherein the high temperature anneal is at least partially performed at 250 degrees Celsius.

13. (previously presented) The method of claim 1, wherein the anneal is performed for a duration that does not alter a critical dimension of the patterned dielectric layer and does not cause a metal extrusion.

14. (previously presented) The method of claim 13, wherein the duration comprises at most three minutes.

15. (previously presented) The method of claim 1, wherein the anneal excludes an application to the patterned dielectric layer of a plasma generated from at least one of: a radio-frequency energy and a microwave energy.

16. (canceled)

17. (previously presented) The method of claim 1, wherein the metal deposition includes a copper deposition.

18. (previously presented) The method of claim 1, wherein the metal deposition comprises at least one of: a barrier deposition and a metal seed layer deposition.

19. (canceled)

20. (previously presented) A method for removing volatile cleanser compounds from a post-etch substrate, comprising:

performing a plasma strip of an exposed low-k dielectric material to remove a photoresist residue after an etch of the material;

performing a wet clean process using a fluorine-based solvent to remove a polymer residue of the plasma strip from the material;

performing an anneal at a pressure of about one atmosphere or less and a temperature of between about 250°C and about 300°C after the wet clean process and prior to a metal barrier deposition to remove a component of the fluorine-based solvent

from the material, wherein the anneal is exclusive of an application of a plasma generated from one or more of: a radio-frequency (RF) radiation and a microwave radiation; and

after an anneal duration of about six minutes or less, stopping the anneal.

21. (previously presented) A method used during fabrication of a semiconductor device, comprising:

patterning a via or a trench, or both, in a low-k dielectric layer comprising organosilicate glass (OSG);

cleaning a polymer residue from a surface of the patterned dielectric layer using a wet clean solvent; and

performing a non-plasma anneal on the patterned dielectric layer at a temperature of about 250°C for a duration of about 45 seconds.

22. (previously presented) The method of claim 21 further comprising performing the anneal at a pressure of about one atmosphere or less.

23. (previously presented) The method of claim 21 further comprising performing the non-plasma anneal to remove a component of the wet clean solvent.

Evidence Appendix

None Submitted

Related Proceedings Appendix

None Submitted